Our Case No.10808/163
Client reference In1228WOUS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR UNITED STATES LETTERS PATENT

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TITLE: METHOD FOR FABRICATING THIN METAL-CONTAINING LAYERS HAVING LOW ELECTRICAL RESISTANCE

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SUBSTITUTE SPECIFICATION UNDER 37 C.F.R. § 1.125

METHOD FOR FABRICATING THIN METAL-CONTAINING LAYERS HAVING LOW ELECTRICAL RESISTANCE

BACKGROUND

[0001] The present invention relates to a method for fabricating thin metal-containing layers having low electrical resistance and, in particular, to thin copper (Cu) interconnects for use in semiconductor components.

[0002] Hitherto, in the fabrication of integrated semiconductor circuits, preferably aluminum layers have been deposited and patterned in respective wiring planes for the realization of interconnects, in which case, in principle, an Al layer has been deposited up to a predetermined thickness and then patterned by means of conventional photolithographic and associated etching methods.

[0003] Increasingly, however, alternative materials are being employed in particular for use in metallization layers of this type in order to comply with the increasing integration density. By virtue of the use of copper, for example, for wiring planes of this type, on account of the significantly lower resistances compared with aluminum, it has been possible to develop integrated circuits which operate at significantly higher speeds and with a lower power consumption. What is disadvantageous, however, in the use of alternative materials of this type, in particular when using copper, is the relatively poor manageability which results from deposition and/or etching problems, for example.

[0004] In order to eliminate problems of this type, the damascene technology illustrated in Figures 1a and 1b, for example, has been developed.

[0005] Figures 1a and 1b show simplified sectional representations for illustrating essential fabrication steps of a conventional damascene method of this type for forming thin metal-containing layers.

[0006] In accordance with Figure 1a, a dielectric layer 2 is situated on a carrier substrate 1, which represents for example an integrated semiconductor circuit in a semiconductor substrate with overlying element layers, a trench for an interconnect that is to be formed later being formed in the said dielectric layer. In subsequent steps, a diffusion barrier layer 3 (liner) and a seed layer 4, enabling or

simplifying growth of a Cu layer 5, are formed both at the surface and in the trench of the dielectric layer 2.

[0007] In accordance with Figure 1b, afterwards, for example by means of a CMP method (chemical mechanical polishing), the layer sequence remaining above the trench is removed and a further diffusion barrier layer 6 is formed as a so-called cap layer.

[0008] In this way, it is possible to fabricate even very finely patterned interconnects with materials that are difficult to manage. What is disadvantageous in this case, however, in particular with feature sizes of less than 0.2 micrometer, is a significant impairment of the electrical conductivity on account of grain size problems within the metal-containing layer 5.

[0009] Figure 2 shows a simplified plan view of a differently patterned interconnect in accordance with a further prior art, as is disclosed for example in the literature reference Q.T. Jiang et al., Proceedings of 2001 IICT Conference, pages 227 to 229. In accordance with this document, the structure-dependent recrystallization represented in Figure 2 was established junction by junction, a metal-containing layer having different grain sizes 5A and 5B being formed in finely patterned regions having, for example, a structure width w1 in contrast to coarsely patterned regions having a structure width w2. In this case, on account of their smaller grain size, the finely patterned regions having a width w1 have a significantly larger resistance than the coarsely patterned regions 5B with their large grain sizes. What is disadvantageous in this case, however, is that, in the finely patterned regions, even at a higher annealing temperature and with a lengthened annealing time, it is not possible to produce the same large grain sizes as in the coarsely patterned regions since the maximum grain size is essentially limited by the geometry of the structures to be filled.

SUMMARY

[0010] Therefore, the invention is based on the object of providing a method for fabricating thin metal-containing layers having low electrical resistance which can be realized simply and cost-effectively. Furthermore, the invention is based

on the object of fabricating thin metal-containing layers having improved electromigration properties.

[0011] According to the invention, this object is achieved by means of the measures of the embodiments described herein.

[0012] In particular by virtue of the formation of a metal-containing starting layer having a first grain size on a carrier material and the subsequent production and movement of a locally delimited thermal region in the metal-containing starting layer in such a way that a recrystallization of the metal-containing starting layer is carried out for the purpose of producing a metal-containing layer having a second grain size, which is enlarged with respect to the first grain size, metal-containing layers having an improved conductivity and improved electromigration properties are obtained.

[0013] Preferably, interconnects are formed in a primary direction and/or in a secondary direction, which is essentially perpendicular to the primary direction, and the movement of the thermal region is carried out essentially in the said primary direction and/or secondary direction or at an angle of 45 degrees to the primary and secondary direction. In this way, the interconnects that are usually arranged orthogonally with respect to one another in a semiconductor circuit can be recrystallized in their respective directions of propagation, thus resulting in enlarged grain sizes and, consequently, reduced conduction resistances and improved electromigration properties. Particularly when the thermal region is moved over the metal-containing starting layer in a manner carried out at an angle of 45 degrees, it is possible to realize a recrystallization particularly simply, rapidly and thus cost-effectively for an entire semiconductor module or semiconductor wafer. Such a process in which the thermal region sweeps over the metal-containing layer to be recrystallized can also be carried out a number of times in this case, thus yielding improved recrystallization results and hence improved electrical properties and also electromigration properties.

[0014] The locally delimited thermal region is preferably produced by means of a fanned-out laser beam, a hot gas, a multiplicity of heating lamps and/or a heating wire, which are lead at a predetermined speed over the metal-containing

starting layer. In the case of such production of the thermal region, which can also take place in a protective gas atmosphere, for example, a recrystallization of the metal-containing starting layer can be carried out particularly effectively and rapidly. In this case, the locally delimited thermal region may be formed for example in strip-type or point-type fashion.

[0015] The metal-containing starting layer may have a metal alloy or a doped metal with an impurity proportion of less than 5%, in which case, during the thermal treatment, the impurity proportions or dopants can outdiffuse to the surface and produce a self-passivating surface layer. In this way, additional passivation steps can be obviated particularly in the fabrication of interconnects by means of a damascene technology.

[0016] In particular when the method is used for forming semiconductor circuits, a temperature of the locally delimited thermal region lies in a range of from 150 degrees Celsius to 450 degrees Celsius, as a result of which the electrical properties of so-called low-k dielectrics, in particular, are not adversely affected. Furthermore, the use of diffusion barrier layers and seed layers makes it possible to bring about an improved crystallization process for the metal-containing starting layer and to reliably prevent an undesirable diffusion of substances that impair the electrical properties of the semiconductor circuit.

[0017] The invention is described in more detail below using exemplary embodiments with reference to the drawing.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] In the figures:

[0019] Figures 1a and 1b show simplified sectional views for illustrating essential fabrication steps in a conventional damascene method;

[0020] Figure 2 shows a simplified plan view for illustrating structurally governed recrystallization properties in accordance with the prior art;

[0021] Figure 3 shows a simplified plan view for illustrating a fabrication method in accordance with a first exemplary embodiment;

[0022] Figure 4 shows a simplified plan view for illustrating a fabrication method in accordance with a second exemplary embodiment; and

[0023] Figure 5 shows a simplified plan view for illustrating a fabrication method in accordance with a third exemplary embodiment.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

[0024] The invention is described below using a Cu layer as metal-containing layer, other metal-containing layers and, in particular, Al, Ag, Pt and/or Au also being able to be used in the same way. Alternative materials of this type for realizing metallization layers are increasingly gaining in importance, in particular in semiconductor technology, since they enable an improved conductivity and, consequently, increased clock rates and also a reduced power consumption.

[0025] However, the problems described in the introduction arise particularly in the case of very small feature sizes of less than 0.1 micrometer (with regard to their thickness or height), a significant increase in resistance commencing in particular on account of the very small grain sizes in the electrically conductive material. Furthermore, such small grain sizes lead to an intensified, but undesirable, electromigration in the direction of the respective interconnects. The advantages of new or alternative wiring materials of this type may be reduced in this way.

[0026] The method according to the invention now shows how usable thin metal-containing layers having low electrical resistance and improved electromigration properties can be fabricated in a simple manner even for very small feature sizes of less than 0.2 micrometer.

[0027] Figure 3 shows a simplified plan view of patterned metal-containing layers or interconnects 5 for illustrating an essential method step in the fabrication of thin metal-containing layers in accordance with a first exemplary embodiment.

[0028] The patterned metal-containing layers 5 have been fabricated for example by means of the damascene technology illustrated in Figures 1a and 1b, identical reference symbols denoting identical or corresponding elements or layers

and a repeated description being dispensed with below. Accordingly, by means of a conventional damascene technology of this type, a diffusion barrier layer 3, a seed layer 4 and a metal-containing starting layer 5A, having a first grain size, may be formed in a dielectric layer 2 or in trenches formed therein, the plan view illustrated in Figure 3 resulting after a CMP method.

[0029] After such a realization of very narrow (e.g. less than 0.1 micrometer) dual damascene Cu interconnects 5, a fanned-out laser beam, for example, for producing a locally delimited thermal region W sweeps slowly along a primary direction x of the interconnects or metal-containing layers 5 and heats the latter to a local temperature within a range of from approximately 150 degrees Celsius to 450 degrees Celsius. The movement (e.g. 1 cm/second) of the temperature front thus produced along the interconnect 5 enables a recrystallization of the small and randomly distributed copper grains from a first grain size 5A to an enlarged second grain size 5C. More precisely, a tendency towards the production of grains that are lengthened in the direction of movement or in the direction of the interconnects 5 results in this case.

[0030] On account of the lengthening of the Cu grains along the interconnects 5, a significantly reduced grain size scattering (grain boundary scattering) results for the electric current or the corresponding free charge carriers. At the same time, this brings about a significantly reduced resistance, which in turn leads to a higher conductivity and improved electromigration properties. In semiconductor circuits, in particular, the power consumption can be reduced and the clock rates can be increased in this way.

[0031] During the laser scanning or while the locally delimited thermal region W sweeps over the metal-containing starting layer 5A with its first grain size, the temperature should not exceed 450 degrees Celsius since a multiplicity of so-called low-k dielectrics, which surround the Cu interconnects 5, for example, do not withstand such temperatures and, moreover, lower temperatures reduce the probability of so-called Cu hillock formation. Furthermore, in the case of such a temperature range, an undesirable outdiffusion of dopants in the semiconductor

material and thus an impairment of the electrical properties of semiconductor elements can be reliably prevented.

[0032] This process is preferably carried out in a protective gas atmosphere comprising N_2, Ar, He or in a vacuum, thereby reducing or preventing an oxidation of the metal-containing layer, for example.

[0033] The seed layer 4 used in the present exemplary embodiment comprises a Cu seed layer, for example, as a result of which the metal-containing Cu initial layer 5A can be formed particularly effectively and simply. Methods for forming the said metal-containing initial layer 5A are conventional PVD or CVD methods, for example, but an electrodeposition or electrochemical deposition method (ECD) may preferably be used. In this case, the seed layer 4 is used as a growth electrode for the metal-containing initial layer 5A with its first grain size.

[0034] As an alternative to the above described copper or the further materials, such as Al, Ag, Pt or Au, for example, for the metal-containing initial layer 5A, it is also possible to use alloys or so called doped metals as the metal-containing initial layer 5A, thereby resulting, as required, in improved electrical properties or a simplified fabrication. Doped metals of this type are, for example, AlCu with 0.5% Cu, AlSiCu with 1% Si and 0. 5% Cu, CuTi, CuIn, CuSn, CuMg, CuAl, CuZr, etc., the dopant concentration essentially being less than 5%.

[0035] Particularly when using such metal alloys or doped metals with an impurity proportion of less than 5%, later passivation steps can be obviated, thereby resulting in a simplification and saving of costs. More precisely, when using such metal alloys or doped metals for the metal-containing initial layer 5A, during the thermal treatment by means of the locally delimited thermal region W, dopants or impurity proportions are outdiffused to the surface, thereby producing a self-passivation surface layer. In this case, it is possible to omit a deposition of the cap layer 6 illustrated in Figure lb, for example, and usually comprising SiN, SiC, BlOK, etc.

[0036] As an alternative to the above described laser heat source for producing a fanned out laser beam, the locally delimited thermal region W may also be produced by means of a hot gas such as e.g. Ar, N_2 or He, which flows out through

a correspondingly shaped nozzle, a heating wire or a multiplicity of heating lamps arranged in an array. The simplest and most cost-effective solution can thus be realized depending on the standard process implemented.

[0037] In this case, the movement of the locally delimited thermal region W which is carried out in the arrow direction is set in a manner dependent on the supplied quantity of energy in such a way as to result in each case in an optimum recrystallization of the metal-containing initial layer 5A having the first grain size to form the metal-containing layer 5C having a second grain size, which is enlarged or lengthened with respect to the first grain size.

[0038] Figure 4 shows a simplified plan view of a patterned metal-containing layer 5 for illustrating a fabrication method in accordance with a second exemplary embodiment, identical reference symbols designating elements or layers identical or corresponding to those in Figures 1 and 3 and a repeated description being dispensed with below.

[0039] In accordance with Figure 4, the metal-containing initial layers 5A with their first grain size are not formed exclusively in a primary direction x, but rather also in a secondary direction y, which is essentially perpendicular to the primary direction x, as they are customarily arranged as interconnects in semiconductor circuits.

[0040] In accordance with an embodiment that is not illustrated, the locally delimited thermal region W can now be moved firstly in the primary direction x and subsequently in the secondary direction y, as a result of which the recrystallization according to the invention to form the enlarged or lengthened second grain sizes in the metal-containing layer 5C is established in the associated interconnect regions.

[0041] In accordance with Figure 4, however, in order to realize this recrystallization more rapidly and more effectively, it is also possible to carry out a scanning process which is carried out at an angle of 45 degrees to the primary and secondary direction x and y, the interconnect regions simultaneously being recrystallized in the primary direction x and also in the secondary direction y and being converted into the lengthened or enlarged crystal sizes of the metal-

containing layer 5C. Accordingly, the movement of the locally delimited thermal region W can be moved not only in the primary direction x or the secondary direction y, but also in a direction which is at an angle (of preferably 45 degrees) thereto, thereby resulting in a particularly effective recrystallization of, in particular, semiconductor wafers. Moreover, it is also possible to effect repeated sweeping-over in the different directions, as a result of which, in some instances, a recrystallization quality can be improved or a more extensive enlargement of the grain sizes can be achieved.

[0042] Consequently, very thin, closely adjacent interconnects having a width of less than 0.2 micrometer can be significantly improved with regard to their conductivity and electromigration properties.

[0043] However, in addition to the improvement of metal-containing initial layers which is based, in particular, on the damascene technology, it is also possible to improve alternatively patterned or non-patterned metal-containing initial layers in this way with regard to their conductivity and electromigration properties.

[0044] Figure 5 shows a simplified plan view for illustrating an essential fabrication step in accordance with a third exemplary embodiment of this type, identical reference symbols designating identical or corresponding elements or layers and a repeated description being dispensed with below.

[0045] In accordance with Figure 5, there is situated on a carrier material a whole area metal-containing initial layer or metallization 5 having a first grain size 5A, which, in contrast to the above-described strip-type locally delimited thermal region W, is now treated with a point-type or circular locally delimited thermal region W. This locally delimited thermal region W is now moved, in accordance with Figure 5, on a volute line once again in such a way as to result in a recrystallization of the metal-containing starting layer 5A for the purpose of producing the metal-containing layer 5C having the second grain size that is enlarged with respect to the first grain size. In this way, even whole-area metal-containing initial layers 5 can be improved with regard to their conductivity and electromigration properties, as a result of which it is possible to form not only

improved metallization planes for semiconductor circuits but also metal-containing layers having improved electrical properties for other areas of application.

[0046] The invention has been described above on the basis of a dual damascene Cu layer as metal-containing initial layer, but it is not restricted thereto and encompasses alternative metal-containing materials and alternative patterning methods in the same way.

[0047] In the same way, the present invention is not restricted to a carrier substrate which comprises a semiconductor circuit, but rather can be formed in the same way on arbitrary other carrier materials on which a very thin electrically conductive layer having low electrical resistance is intended to be formed.

[0048] Moreover, the above-described thermal treatment also need not be applied to an uncovered metal-containing initial layer, rather it is also possible for one or more protective lavers to lie above or below the metal-containing initial layer to be recrystallized. Accordingly, in particular, the cap layer 6 and intermetal dielectrics (not illustrated) may already be formed before the thermal treatment.

[0049] Furthermore, the above-described thermal treatment can also be carried out before the Cu CMP step in accordance with Figure 1a, or else in any desired combination, i.e. before/after the Cu CMP step or after cap layer 6 and further intermetal dielectrics.